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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,084	03/10/2004	Tony H. Ho	MR1035-1427	2320

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EXAMINER	
FARAHANI, DANA	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/796,084	HO, TONY H.	
	Examiner	Art Unit	
	Dana Farahani	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation that of "said flat surface ...comprises a concave middle" must be shown or the features canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 1 is objected to because of the following informalities: it states a semiconductor die "uplying" (sic: overlying) said top surface. Appropriate correction required.

3. Claim 18 is objected to because of the following informalities: it contains the phrases "said first plurality of solder joints" and "said fourth plurality of solder joints". First plurality of solder joints and fourth plurality of solder joints need to be defined first in the claim, and are not to be referred to as if they have been defined, while in fact they have not.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-19 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1-17, claim 1 states an "electrically substrate" and "therefrom", which is not clear as to what it is referring to. Also, claim 5 recites the limitation "said flat surface" of claim 1; claim 6 recites "on third array" of claim 1; claim 8 recites "said flat surface of said fourth plurality of solder joints" of claim 1; claim 9 recites "said flat surface implemented on said first plurality of solder joints" of claim 1; claim 10 recites "said third plurality of solder joints" of claim 1; claim 12 recites "said third plurality of solder joints and said fourth plurality of solder joints" of claim 1; and claim 15 recites "the number of semiconductor dies" of claim 1

(claim 1 indicates the presence of only one semiconductor die). There is insufficient antecedent basis for those limitations in the above noted claims.

Regarding claims 18 and 19, claim 18 states "at least one semiconductor die" (singular) and then immediately states "a printed circuit board underlying said dies" (plural). It is not clear as to how many dies it is referring to.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-6 and 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang (US Patent 6,717,253) in view of Roldan et al. hereinafter Roldan (US Patent 6,005,292) further in view of Kajiwara et al., hereinafter Kajiwara (US Patent Application Publication 2003/0001286).

Regarding claims 1-2, 5, and 11, Yang discloses in figure 2 a semiconductor packaging structure comprising a substrate 202 having a top surface and a bottom surface; a semiconductor die 205 up-lying the top surface; and

a first array comprising a first plurality of solder joints 215, mounted on the die surface and projecting downwardly.

Yang does not disclose the solder joint of a second array comprising flat surfaces at the front edges of a second plurality of solder joints, mounted on the top surface, integral with the first array, therefrom, connecting the die surface and the top surface;

and a group of solder paste located between the first array and the second array, therefrom, the first plurality of solder joints and the second plurality of solder joints having a higher melting point than the solder paste.

Roldan discloses in figure 2, conductive bump arrays 34 and 44 of the electronic devices 30 and 36 are connected together, as can be seen in the figure. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a second array of solder joints, mounted on the top surface of the substrate of the Ward's structure in order to make a more secure connection between the die and the substrate of the structure.

Roldan does not disclose a group of solder paste between the first and second array, and the first and second array comprising a flat surface, and the first plurality of solder joints and the second plurality of solder joints having a higher melting point than the solder paste.

Kajiwara discloses in figure 1, first and second array of solder joints, 7 and 8, respectively, wherein the second array comprises a flat surface (see figure 2A), and a group of solder paste 9 between the first and second array. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the second solder joint arrays with flat surfaces to increase the contact area between the first and second array and make a good connection between them. Although, Kajiwara does not expressly disclose the first plurality of solder joints and the second plurality of solder joints having a higher melting point than the solder paste, it would have been obvious to make the paste to have a melting point lower than the

melting point of the solder joints, so when the curing of the paste is done, it does not effect the formation of the connection between the first and second array. Also, note that at integral process of the Kajiwara, the solder joints were not melted while the solder paste were (see page 5, paragraph 50, the last three lines).

Regarding claims 3-4, 6, 12-14, 18 and 19, Yang discloses a PCB, not shown in figure 2 but is present below substrates 201 and 202 (see column 3, line 46) underlying the substrate; and a third array comprising a third plurality of solder joints 212, mounted on the bottom surface and projecting downwardly. Although Yang does not disclose the third array having a flat surface, a fourth array of a plurality of solder joints on the printed circuit board and a group of solder paste between the third array and the fourth array, the Roldan and Kajiwara references render obvious these limitations, as discussed above with respect to rejection of claim 1.

Regarding claim 15, there is another die 201 in the Yang reference.

Regarding claims 16 and 17, the solder joints on the bottom surface would have been heading in correspondence with the solder joints on the top surface, since the solder joints on the top surface would have been located on pads 224.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER